SELF-TIMED READ AND WRITE

ASSIST AND RESTORE CIRCUIT

ABSTRACT OF THE DISCLOSURE

A read and write assist and restore circuit for a memory device includes a first device, which is responsive to a potential on a bit line such that the potential on the bit line activates the first device. A second device is driven by the first device such that when the first device is activated, a change in the bit line potential is reinforced with positive feedback by the second device during a wordline active period to enable write-back of data lost as a result of threshold voltage fluctuations in memory cell transistors coupled to the bit line.